

### **REMARKS**

Claims 1, 2 and 5-8 are pending in the application.

Claim 8 has been rejected under 35 U.S.C. 112, second paragraph. This claim has been amended to overcome the rejection under 35 U.S.C. 112, second paragraph.

Claims 1, 2 and 5-7 are rejected under 35 U.S.C. 103 as being unpatentable over Hong (5,445,983) in view of Wong (6,091,634). The Examiner states that Hong teaches in Fig. 1A the tunneling insulator 36 disposed below the floating gate 42 and gate 24 of the select transistor.

Claims 1, 2, 7 and 8 have been amended to more clearly distinguish over the prior art. As disclosed by Hong (Fig. 1A) the tunneling gate oxide layer 36 is not disposed directly below the gate 24 of the select field effect transistor.

The amended claims have antecedent support on page 15, line 15 to page 16, line 10, of the specification, and Figs. 7A-7I of the drawings. As disclosed in the specification, polysilicon film 6, which is to be a portion of a floating gate of the memory cell transistor MTr and a gate of the select transistor structure, is stacked on the tunnel gate oxide film 5.

Accordingly, claims 1, 2 and 5-8 are allowable over the art.

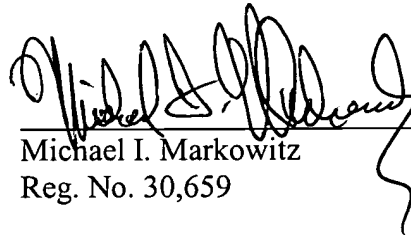
### **CLOSING**

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that independent claims 1, 2, 7 and 8 are in condition for allowance, as well as those claims dependent therefrom. Passage of this case to allowance is earnestly solicited.

However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper, not fully covered by an enclosed check, may be charged on Deposit Account 50-1290.

Respectfully submitted,



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